

Docket No.: YHK-0110

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Jang Hwan CHO and Won Sik YOON

Serial No: 10/743,289

Filed: 12/23/2003

Confirmation No.: 7859

Group Art Unit: 2821

Examiner : A. Minh D.

Customer No.: 34610

For: ENERGY RECOVERING APPARATUS AND METHOD FOR PLASMA DISPLAY PANEL

U.S. Patent and Trademark Office
Customer Window, Mail Stop Amendment
Randolph Building
401 Dulany Street
Alexandria, Virginia 22314

Dear Sir:

Transmitted herewith is an Amendment and/or Reply in the above identified application.

- ☐ No additional fee is required.
☒ Also attached: Extension of Time fee

The fee has been calculated as shown below:

	NO. OF CLAIMS	HIGHEST PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	14	20		x \$50.00 =	\$
Independent Claims	2	3		x \$200.00=	\$
If multiple claims newly presented, add \$360.00					
Fee for extension of time					1,020.00
TOTAL FEE DUE					\$1,020.0

- ☐ Please charge my Deposit Account No. 16-0607 in the amount of \$____. An additional copy of this transmittal sheet is submitted herewith.
- ☒ A check in the amount of \$ 1,020.00 (Check #15497) is attached.
- ☒ The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 16-0607, including any filing fees under 37 C.F.R. 1.16 for presentation of extra claims and any patent application processing fees under 37 C.F.R. 1.17.

Respectfully submitted,
FLESHNER & KIM, LLP

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Date: July 25, 2005

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PANEL

REQUEST FOR RECONSIDERATION

U.S. Patent and Trademark Office
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Randolph Building
401 Dulany Street
Alexandria, Virginia 22314

Sir:

In reply to the Office Action dated January 25, 2005, the period for reply being extended from April 25, 2005 to July 25, 2005 by a Petition for a Three-Month Extension of Time filed herewith, reconsideration of the rejection for the reason set forth below is respectfully requested.

Concurrently filed with this reply is an Information Disclosure Statement. Further, this application is related to co-pending Patent Application Nos. 10/416,286, 10/743,284 and 10/824,417. Hence, all references cited in those applications should be considered during the prosecution of this application.

The allowance of claims 2, 3, 5-8 and 10-14 is greatly appreciated. However, it is respectfully submitted that claims 1, 4, and 9 is patentably distinguishable over the cited reference.

In particular, claims 1, 4 and 9 stand rejected under 35 U.S.C. §102(e) over Lee et al. (U.S. Patent No. 6,680,581). This rejection is respectfully traversed.

Lee et al. fails to disclose or teach all the claim features and the combination thereof of independent claims 1 and 9, as required under Section 102. Lee et al. fails to disclose “switching devices for shutting off a path between the voltage source and the second inductor in a state in which energy has been stored in the second inductor to derive an inverse voltage into the second inductor and allowing said inverse voltage to be applied to the panel” and the combination thereof, as recited in independent claim 1 or “shutting off a path between the voltage source and the second inductor in a state in which an energy has been stored in the second inductor using the switching devices to derive an inverse voltage into the second inductor and applying said inverse voltage the panel” and the combination thereof, as recited in independent claim 9.

Independent claims 1 and 9 broadly recite the features disclosed in an embodiment. For example, in a non-claim limiting embodiment of the specification, in time period T3 of Figure 8, the transistors Q1-Q4 are turned off to shut off a path between the voltage source, e.g., voltage source V1 and/or voltage source V2. The inverse voltage is applied to the panel and such inverse application of the voltage is illustrated in the timing signal I_{L2} during the time period T3. Further, Figure 11 illustrates the current path during this time period.

During the time period between t_0 and t_1 (MODE 1) of Figure 3 (Lee et al.), the inductor current I_{L1} reaches a peak but during the inverse polarity, i.e., from peak to 0, between the time periods t_1 and t_2 (MODE 2), the transistors S1 and S2 are turned on such that the voltage V_s is applied to the panel capacitor C_p . In other words, during MODE 2 of Lee et al., the application

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Amdt. dated JULY 25, 2005

Reply to Office Action of January 25, 2005

of inverse polarity, which is shown in the decreasing of the current I_{L1} , is prevented from being applied and the voltage V_s is applied to the panel capacitor, which is opposite of the claim 1 and 9 features. Hence, Lee et al. teaches the opposite of the claimed invention, and cannot disclose or teach all the claimed features.

Lee et al. fails to disclose all the claimed features and the combination thereof. Hence, withdrawal of this §102 rejection is respectfully requested.

In view of the foregoing amendments and remarks, it is respectfully submitted that this application is in condition for allowance. Favorable consideration and prompt allowance are earnestly solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this, concurrent and future replies, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,
FLESHNER & KIM, LLP

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Please direct all correspondence to Customer Number 34610